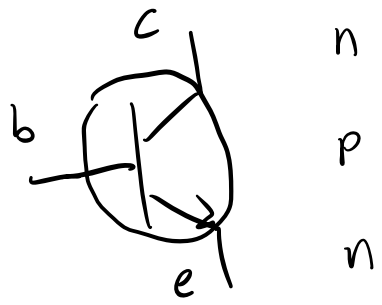
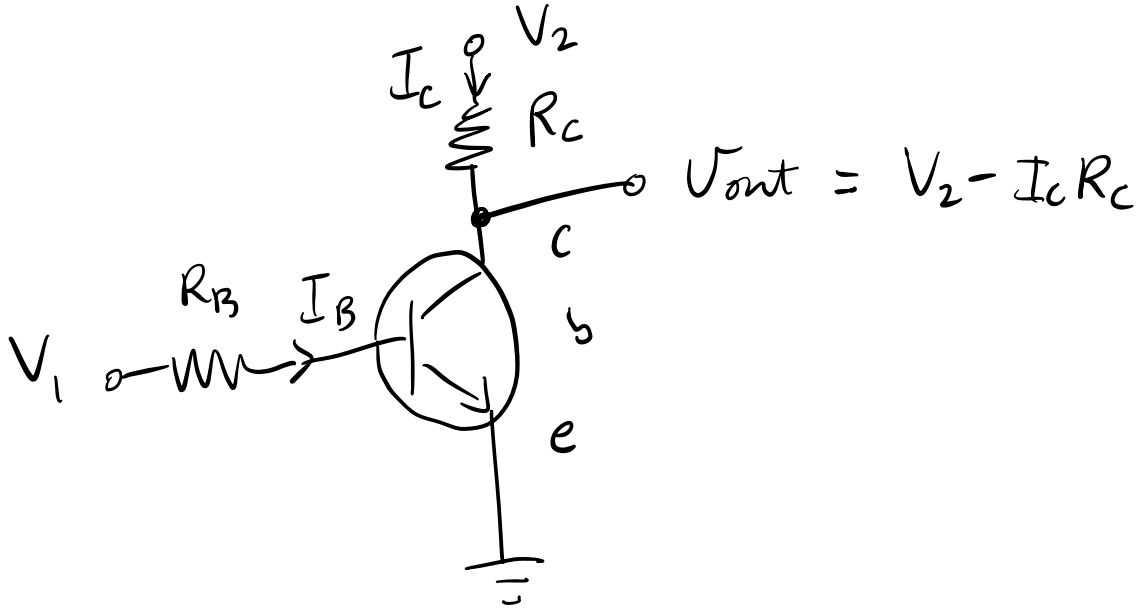
PHYS 231 - Dec. 4, 2023

Submit final project lab notebook at end of lab on Thursday, Dec. 7.

Last Time: npn BJT



Transistor Current Switch



$V_1 < 0.7\,V$, $I_C = 0$ $\Rightarrow$ $V_{out} = V_2$

$V_1 > 0.7\,V$, $I_C \neq 0$ $\Rightarrow$ $V_{out} \approx 0$

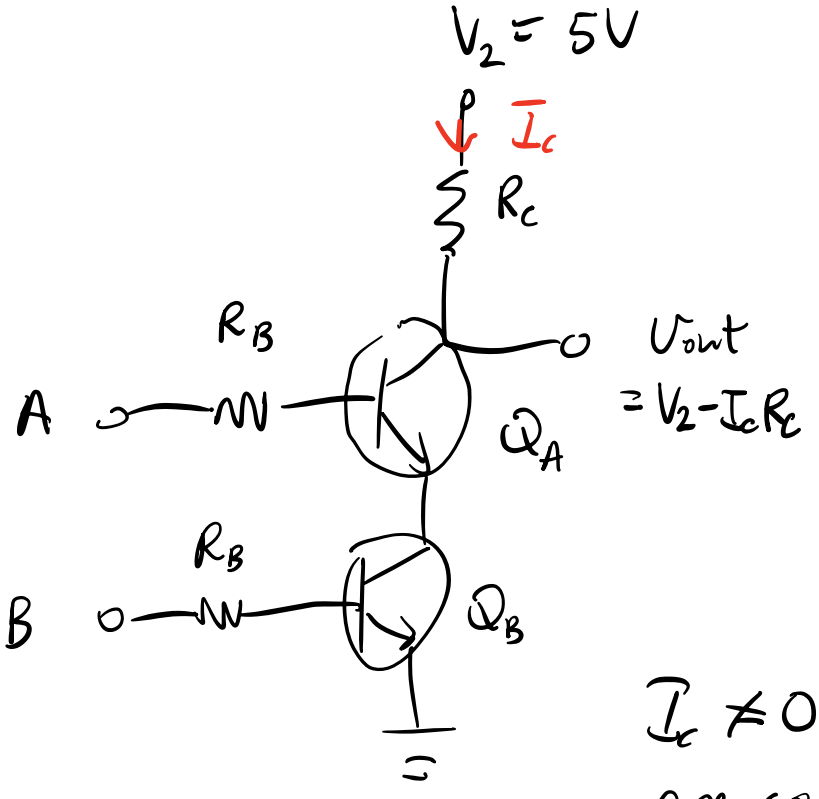
If we set $V_2 = 5\,V$...

This circuit acts as a NOT gate

V_1	V_{out}
LO	HI
HI	LO

How to construct other gates?

Consider a series combination of two transistors.

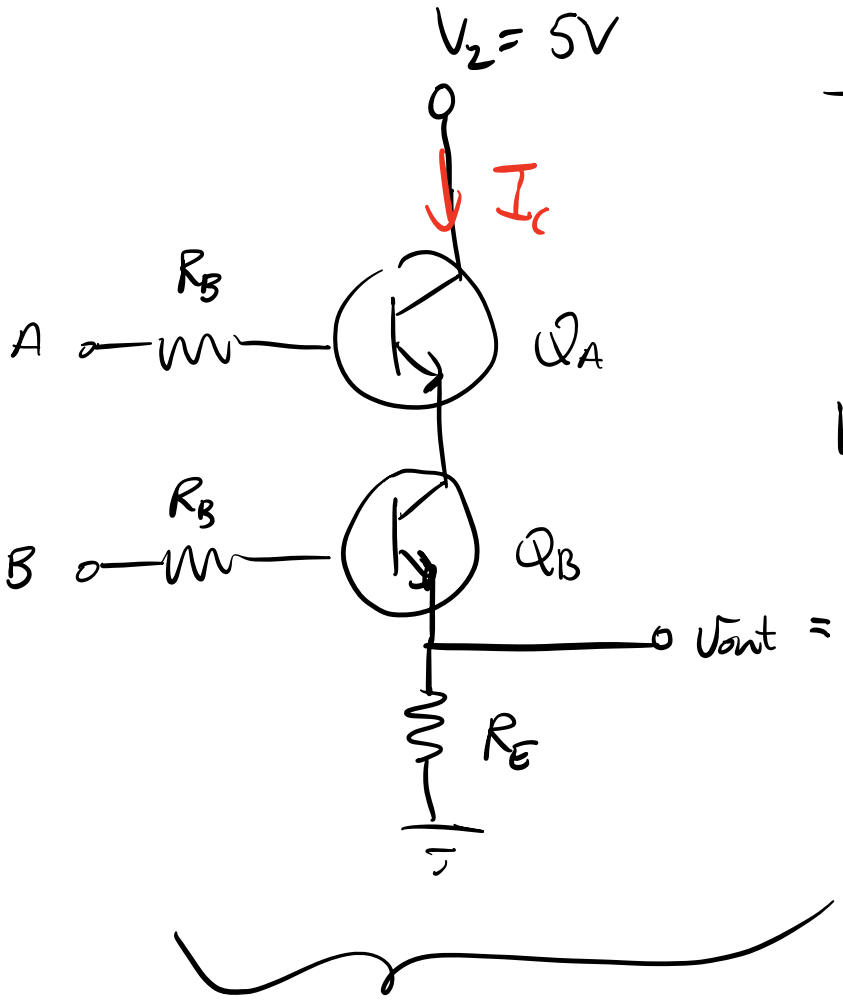


A	B	Q_A	Q_B	I_C	V_{out}
0	0	OFF	OFF	0	1
0	1	OFF	ON	0	1
1	0	ON	OFF	0	1
1	1	ON	ON	$\neq 0$	0

$I_C \neq 0$ only when both Q_A & Q_B are conducting.

Transistor implementation of a NAND gate.

To make an AND gate, consider moving the output.

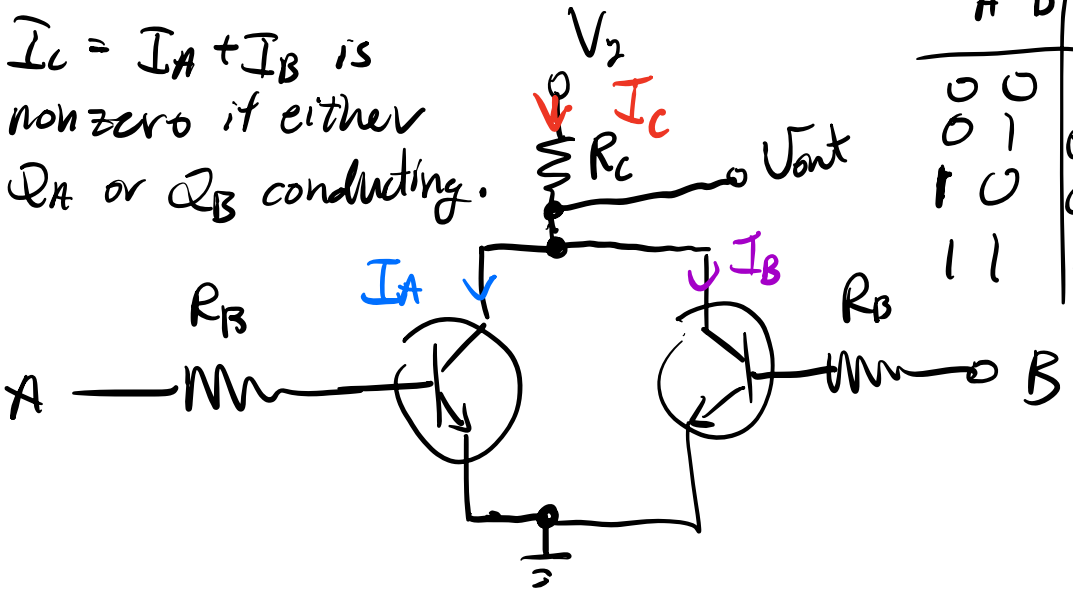


A	B	Q_A	Q_B	I_C	V_{out}
0	0	OFF	OFF	0	0
0	1	OFF	ON	0	0
1	0	ON	OFF	0	0
1	1	ON	ON	$\neq 0$	1

AND gate.

Let's try a parallel comb. of transistors...

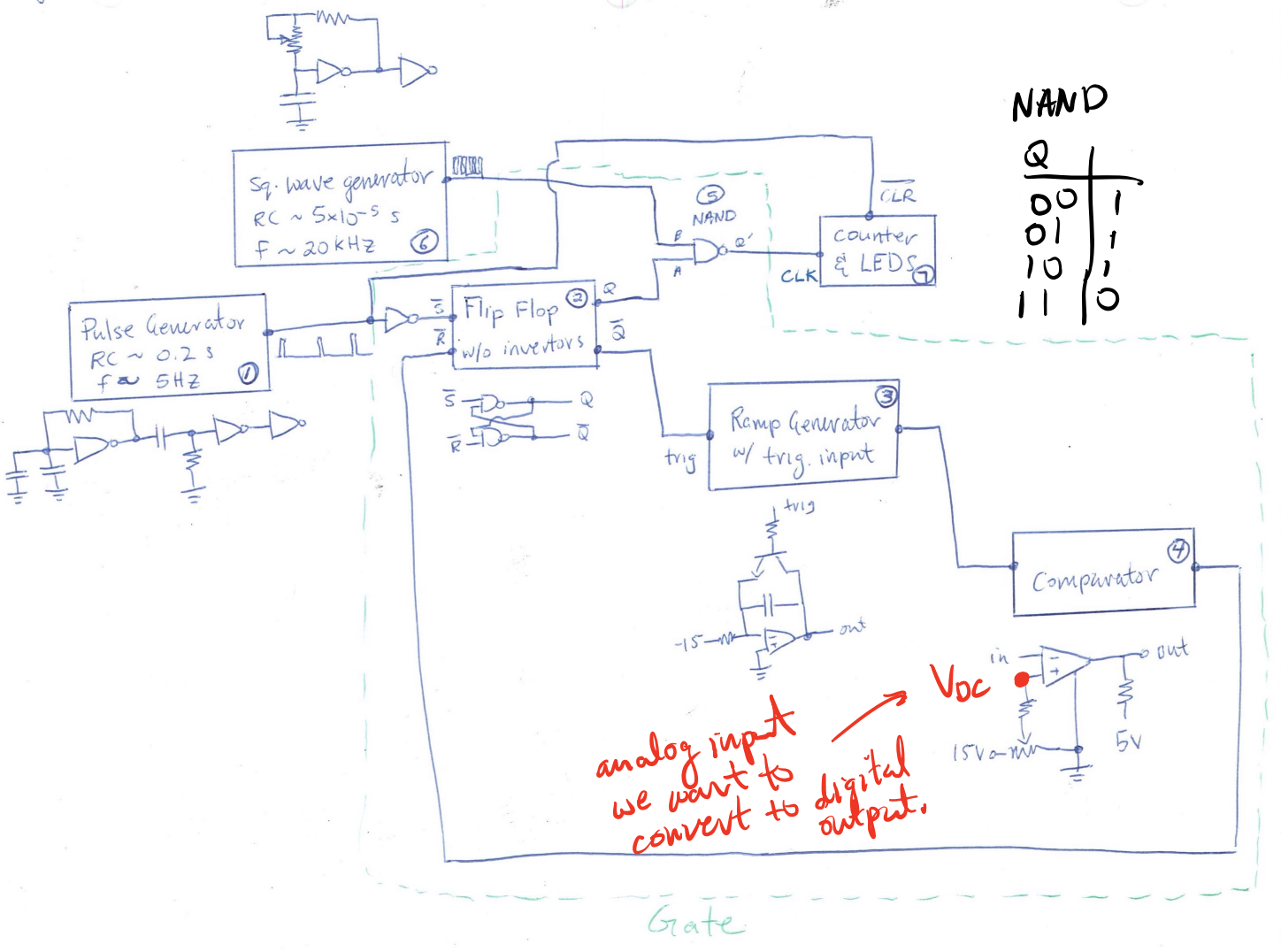
$I_C = I_A + I_B$ is nonzero if either Q_A or Q_B conducting.



A	B	Q_A	Q_B	I_A	I_B	V_{out}
0	0	OFF	OFF	0	0	1
0	1	OFF	ON	0	$\neq 0$	0
1	0	ON	OFF	$\neq 0$	0	0
1	1	ON	ON	$\neq 0$	$\neq 0$	0

NOR gate.

ADC Block Diagram



NAND

Q	
00	1
01	1
10	1
11	0

Goal of ADC is to output a binary (digital) representation of an analog DC voltage.

If the V_{DC} is, for example, 5.3V, want to output:

5 ; 3

0101 | 0011

0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9

Need 53 clock pulses to be passed to counter. Once reach desired no. of counts, block further clock pulses from reaching counter so that we read a stable output. Keep this state until a reset pulse clears the counter.

① Assume that counter just cleared by a reset pulse.

② $\overline{S}$ is HI, but was just pulsed LO. $\Rightarrow Q=1, \overline{Q}=0$

③ Since $\overline{Q}=0$, transistor switch is <u>not</u> conducting & ramp gen. is producing a ramp.

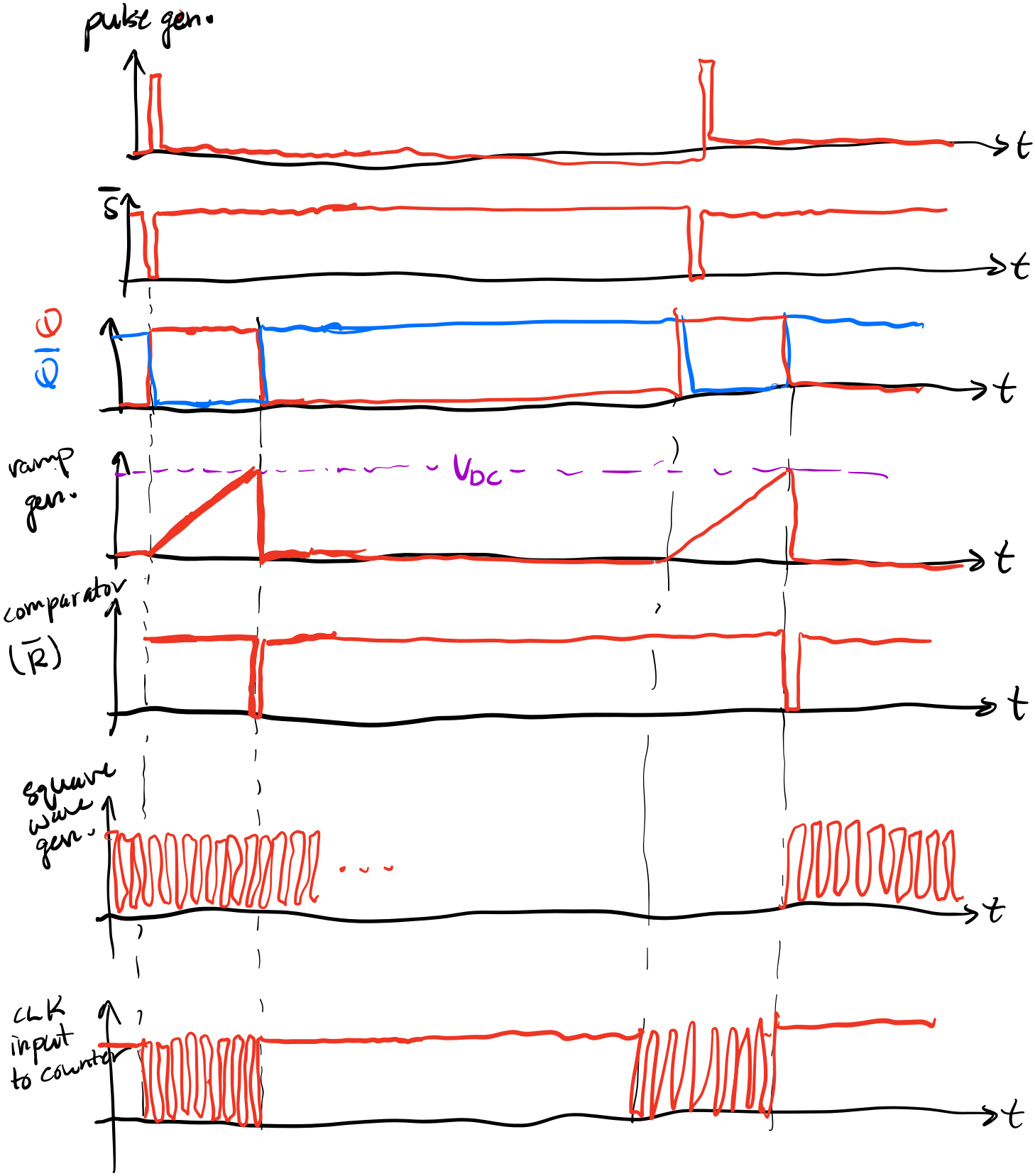
④ Initially, ramp input is less than V_{DC}. ∴ comparator output is HI.

⑥ Squarewave continuously outputs stream of square waves.

Initially, since $Q=1$, the NAND gate ⑤ passes clock pulse to counter & counter is actively counting

④ Eventually, the ramp output reaches V_{DC} which causes the comparator output HI → LO.

② LO comparator output [$\overline{R}$] causes flip to change state $(Q, \overline{Q}) \rightarrow (0, 1)$


pulse gen.
t
$\bar{S}$
t
Q
$\bar{Q}$
t
ramp gen.
V_{DC}
t
comparator
($\bar{R}$)
t
square wave gen.
t
clk input to counter
t

③ Now $\overline{Q} = 1$ which makes transistor conducting s.t. ramp. generator outputs zero.

④ Since ramp is zero, comparator output is Hl again.

⑤ Since $Q = LO$, output of NAND is always Hl.
∴ Clock pulse not passed to counter
∴ counter output is stable.